THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

Quarterly Report #12

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by the

Center for Integrated MicroSystems
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan
48109-2122

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Thin-Film Intracortical Recording Microelectrodes

Summary

The goal of this contract has been to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes have 64 sites, of which eight can be selected for simultaneous use by the external world. On one of the probe designs (PIA-2B/3B), the neural signals are buffered and then passed directly off chip, whereas on the other (PIA-2/-3) the signals are amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) versions of these probes are being developed.

During the past quarter, we have begun a concerted effort to understand the chronic behavior of thin-film recording sites and its relationship to site processing, position, and design. Cleaning procedures are being explored via a series of chronic implants along with experiments investigating site position and size with respect to recording performance. Edge-mounted sites have recently shown high-quality recording performance to beyond 70 days in contrast to the much more limited lifetimes typically seen for sites positioned in the center of the flat probe substrate. A series of recording probes having edge- and center-positioned sites has been fabricated and are now ready for implantation. These will allow a direct comparison with the two placements as well as a comparison with microwire electrodes.

The design of our 64-site 8-channel recording probe, PIA-2B, has been iterated during the past quarter to improve its performance. CMOS pass-gates have been added to replace the NMOS switches used on the previous design, and closed-loop amplifiers have been added to replace the previous buffers. The new design is ready for fabrication during the coming term. In addition, we have developed a mounting/interconnect interface for our 96-site buffered active probe. The interface provides an interface with the outside world using Omnetics NANO connectors. These connectors provide leads on 25mil centers. These buffered probes have been provided to an external investigator (Gyorgy Buzsaki) and used successfully to record from rat hippocampus.

A high-performance recording amplifier for use on the active probes has been designed and thoroughly simulated. The amplifier is immune to process-induced threshold variations with a gain of 100 between 46Hz and 14kHz, a power dissipation of 49µV, a dc gain of unity, and a simulated input-referred noise level of 2.6µVrms. We hope to fabricate this amplifier during the coming term. Many of the components needed for a leadless telemetry interface to these probes have now been fabricated and are being evaluated. A design for the analog-to-digital converter needed for this interface is also being explored.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should also be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the preserving the viability of the sites in-vivo (preventing tissue encapsulation of the sites) and with the probe output leads, both in terms of their number and their insulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the meg-ohm impedance levels of the sites while maintaining lead flexibility.

Our solution to the lead problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of over 100, impedance levels are reduced by four orders of magnitude, and the probe requires only three leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing has been developed (PIA-2B) along with a high-end multiplexed probe that includes gain

(PIA-2). During the past quarter, we have begun a serious effort to understand the chronic behavior of thin-film recording sites and its relationship to site position and design. Cleaning procedures have been explored along with experiments investigating site position and size with respect to recording performance. The design of our 64-site 8-channel recording probe PIA-2B has been iterated to improve its performance and we have developed a mounting/interconnect interface for our 96-site active probe. A high-performance recording amplifier for use on the active probes has been designed and components for use in a telemetry interface to the probes have been developed. Work in these areas is discussed in the following sections.

2. Chronic Recording with Passive Probes

Although we have tried to maintain adequate procedures for chronic implantation for some time and have often sustained successful neural recordings for periods of several months, we have more often experienced a gradual reduction of signal amplitudes and an accompanying increase in site impedance. CNCT users have also experienced similar difficulties using our devices. The general literature has many references to this 'protein fouling' problem, which is thought to be the factor presently limiting the lifetime of sites in-vivo. This problem is thus the principal subject of our of our NCRR-funded CNCT research projects as well as the NPP recording program. Two projects are currently being jointly carried out in this area by our NPP contract efforts and the CNCT Rational Design project. One project has to do with making sure that the probe cleaning procedures used prior to chronic implantation are adequate, and the other explores fouling as a function of site design. The cleaning issue noted below addresses only occasional problems, but the sensor fouling issue is a very routine finding.

Tests of probe cleaning procedures:

As mentioned in the previous quarterly report, we have been concerned over whether we are really achieving complete removal of residual etchants/organics left over from the probe processing/assembly process prior to implantation. A lack of complete cleaning, we believe, has contributed to occasional adverse tissue reactions that we have seen in some of our histology. To better understand this issue we have implanted three animals, each with six probe implants. One of the implants (a four-shank probe) was cleaned using normal procedures and had our usual high-temperature chemical-vapor-deposited oxide (HT-CVD) for its outer dielectrics. A second probe had similar dielectrics but in additional to the normal cleaning steps was cleaned more rigorously using the following steps:

- Ammonium hydroxide, 30% hydrogen peroxide, water (1:1:5), 5 min. at 80 °C,
- Rinse with deionized water, Hydrochloric acid, 30% hydrogen peroxide, water (1:1:5), 5 min. or 20 min. at 80 ° C, and
- Rinse with deionized water.

In addition, third implant was cleaned only with the above rigorous procedure. The final three implants were cleaned in a manner identical to the first three but used low

temperature oxide (LTO) outer dielectrics. These animals will be sacrificed after 3 weeks implantation. The tissue will then be harvested and examined histologically for any adverse tissue reactions.

Site design for Chronic Implantation:

During the past quarter, we have implanted one guinea pig ("Bash") with the single shank edge-site design shown in Fig. 1 in the inferior colliculus (IC). In addition, the animals reported in the previous quarterly report have now all been euthanized. One of them, "Plug," which was also implanted with the edge-site design in the IC, was responding nicely for several weeks (see Fig. 2) when the responses disappeared along with the acoustically-driven background activity. We think the electrode suddenly moved out of the IC since this particular probe design had a rather thick ribbon cable that could have placed higher than normal stress on the implant site. The impedances remained fairly constant except for Ch14 which increased considerably between day 70 and day 72. This increase also corresponds to the time we think that the electrode moved and we stopped getting driven responses. For "Bash" we have attempted to get around this problem by better stabilizing the implant site.

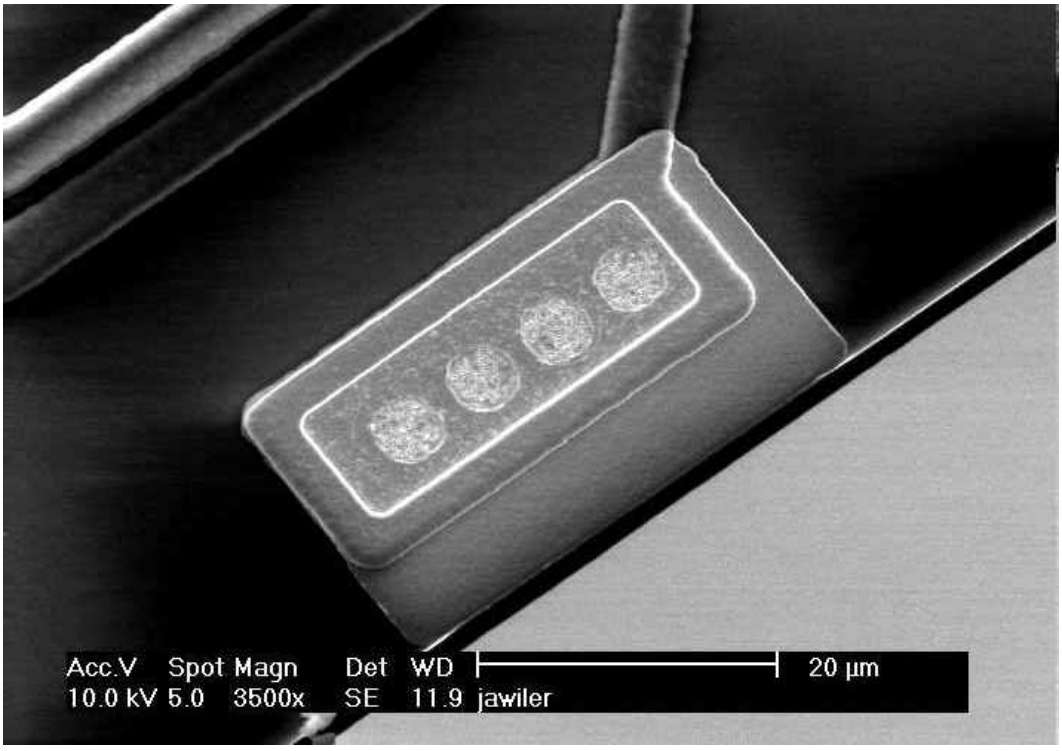


Fig. 1: SEM of edge site.

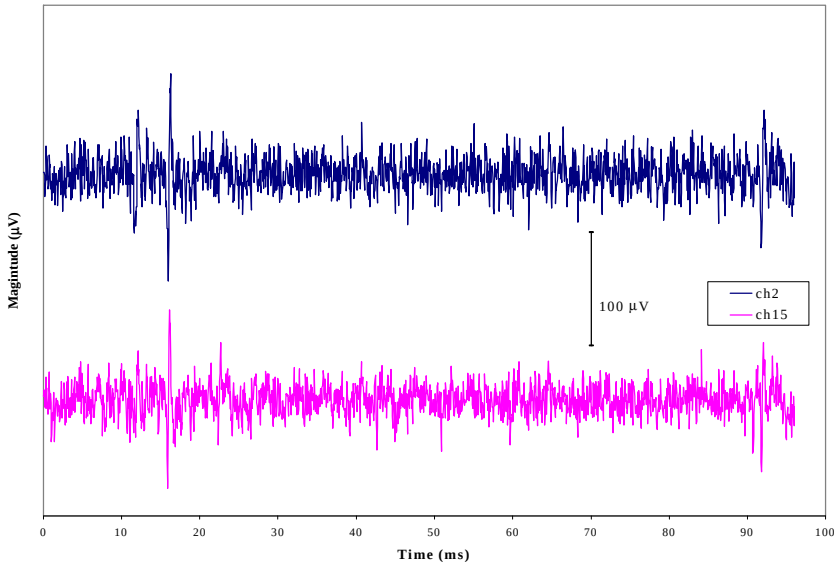
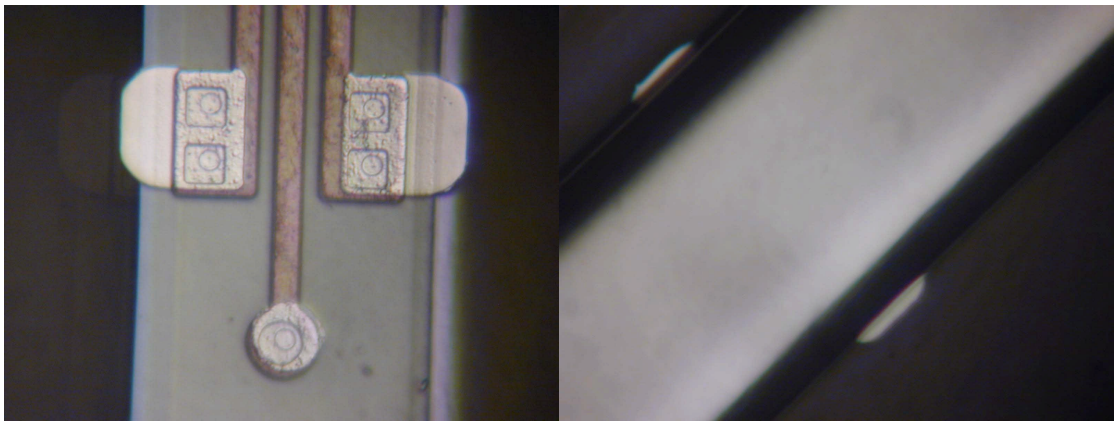


Fig. 2: Recordings taken from Plug on day 70 (channels 2 and 15 are adjacent sites).

3. Probe Design for Chronic Recording

During the past quarter, a set of chronic recording probes has been fabricated. These probes will help address some of the above questions regarding the nature of the tissue/electrode interface and the viability of long-term recordings. We will determine a baseline longevity and stability of chronic cortical recordings with these probes, and explore the hypothesis that the mechanical cleaning of sites due to small electrode movements contributes to longer periods of successful recording.

The probes have sites which are likely to be exposed to small tissue movements due to their location either at the shank tip or overhanging the edge of the shank (Figs. 3 and 4). The sites are located in close proximity to standard 177 µm sites, so that both types of site can record from the same neuron and comparisons of recording lifetime can be made. The probes have integrated silicon ribbon cables which are bonded to 16-channel Omnetics percutaneous connectors. These experiments will also provide additional chronic testing of the silicon ribbon cables. In addition, the implants will provide useful information about experimental procedures in chronic preparations. Chronic implantation of the probes is expected to begin in the next two weeks. The larger sites on these probes are also intended to mimic microwires. Microwire implants in the same preparations will also be used to allow direct comparison to the thin-film sites.



(a) (b)

Fig. 3: Photograph of probe from front (a) and back (b) showing 5µm overhang of sites. The backsides of the sites are insulated with dielectrics.

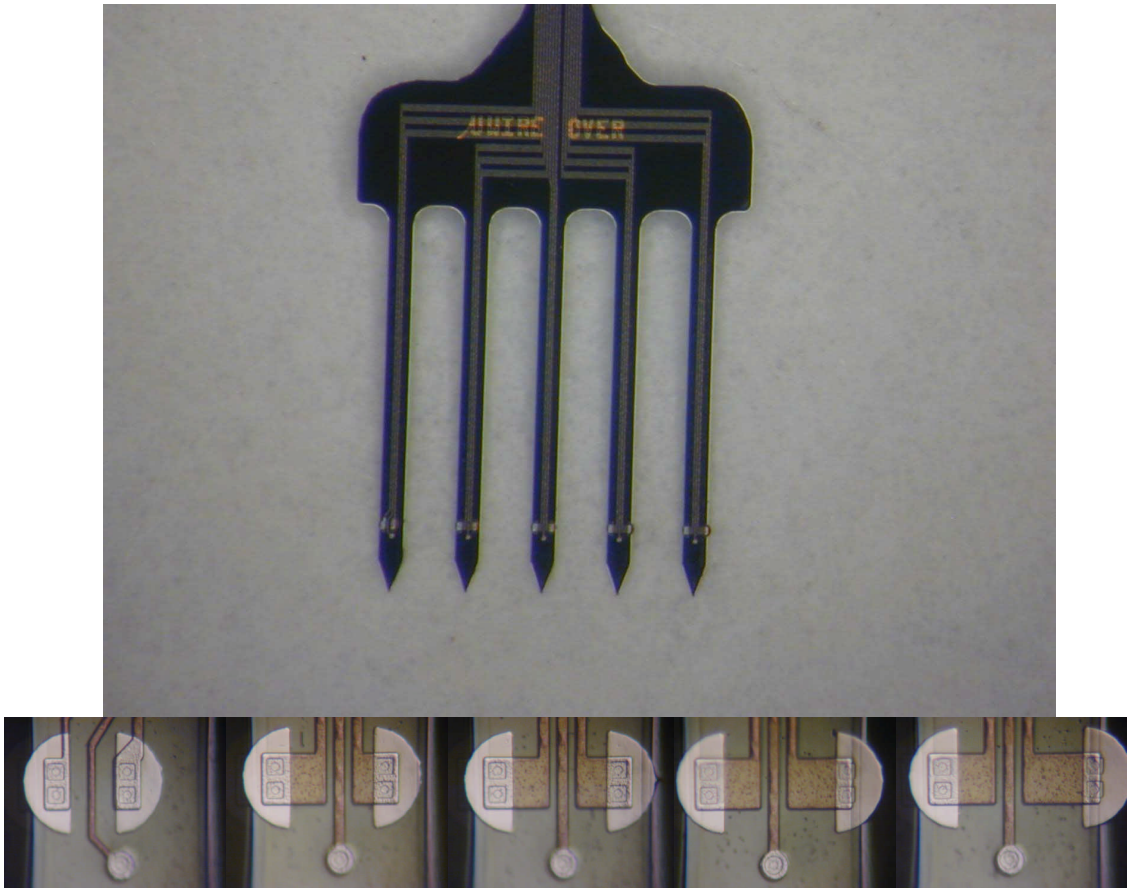


Fig. 4: Photograph of a probe with site overhang. This probe is designed determine whether lateral site location (including overhang) influences the longevity of recording. A control site is located at the shank edge with 5µm overhang, while the second site is displaced laterally in 10µm increments between successive shanks. A standard 177µm^2 center-located site is included for comparison. The sites on a given shank are close enough that we expect to record simultaneously from the same unit, establishing a direct comparison for the implant duration.

4. Development of a 64-Site Eight-Channel Non-Multiplexed Recording Probe (PIA-2B)

During the past quarter, the PIA-2B mask set has been updated to include the changes outlined in the last quarterly report. Full CMOS pass-gates were used in place of separate NMOS and PMOS switches in the buffer bypass circuit. In addition, the signal leads were routed into the circuit area in metal instead of polysilicon to eliminate the danger of shorting by polysilicon streamers along the oxide step. A version of this 64-site 8-channel probe with closed-loop amplifiers in place of buffers is also being incorporated into the mask set.

In addition to the modified PIA-2B probe, several other designs are being included in the current active mask set. A front-end-selected probe intended for chronic use is being designed, and a second implementation of a front-end-selected probe will be included for evaluation. This design utilizes a different scheme for cross wiring the inputs and outputs of the selector and may allow a significant area savings. Probes which include DC input stabilization through input clamp transistors and arsenic implanted polysilicon resistors are also being included for a side-by-side evaluation of these schemes.

Fabrication of these active probes will begin in the coming month.

5. Development of a 96-Site Buffered Recording Probe

Progress on a 96-site buffered recording probe has been described in past reports. The probe has now been tested in-vitro and in-vivo is functioning well. Dr. Gyorgy Buzsaki of Rutgers has done preliminary testing of the probe with nine bonded sites and has obtained satisfactory results recording in rat hippocampus. He is anxious to begin working with a fully bonded probe. In order to accommodate the unusually high lead count, a custom printed circuit board has been designed and fabricated. This board utilizes minimum line widths (3 mil) at the probe back end, which tapers up to a 25 mil pitch to mate with 32- and 35-pin Omnetics nano-connectors. High yield has been achieved in the bonding process, although it is fairly labor intensive.

A probe/PC board/connector assembly is shown in Fig. 5. We expect this probe to be an extremely useful tool for researchers who wish to record simultaneously from a large number of sites. The on-chip buffering reduces noise and eliminates the need for what would be an impossibly large unity-gain headstage. Yet, the significant bottleneck in terms of off-chip interconnect and bonding labor vividly illustrates the importance of our continued development of multiplexed probes.

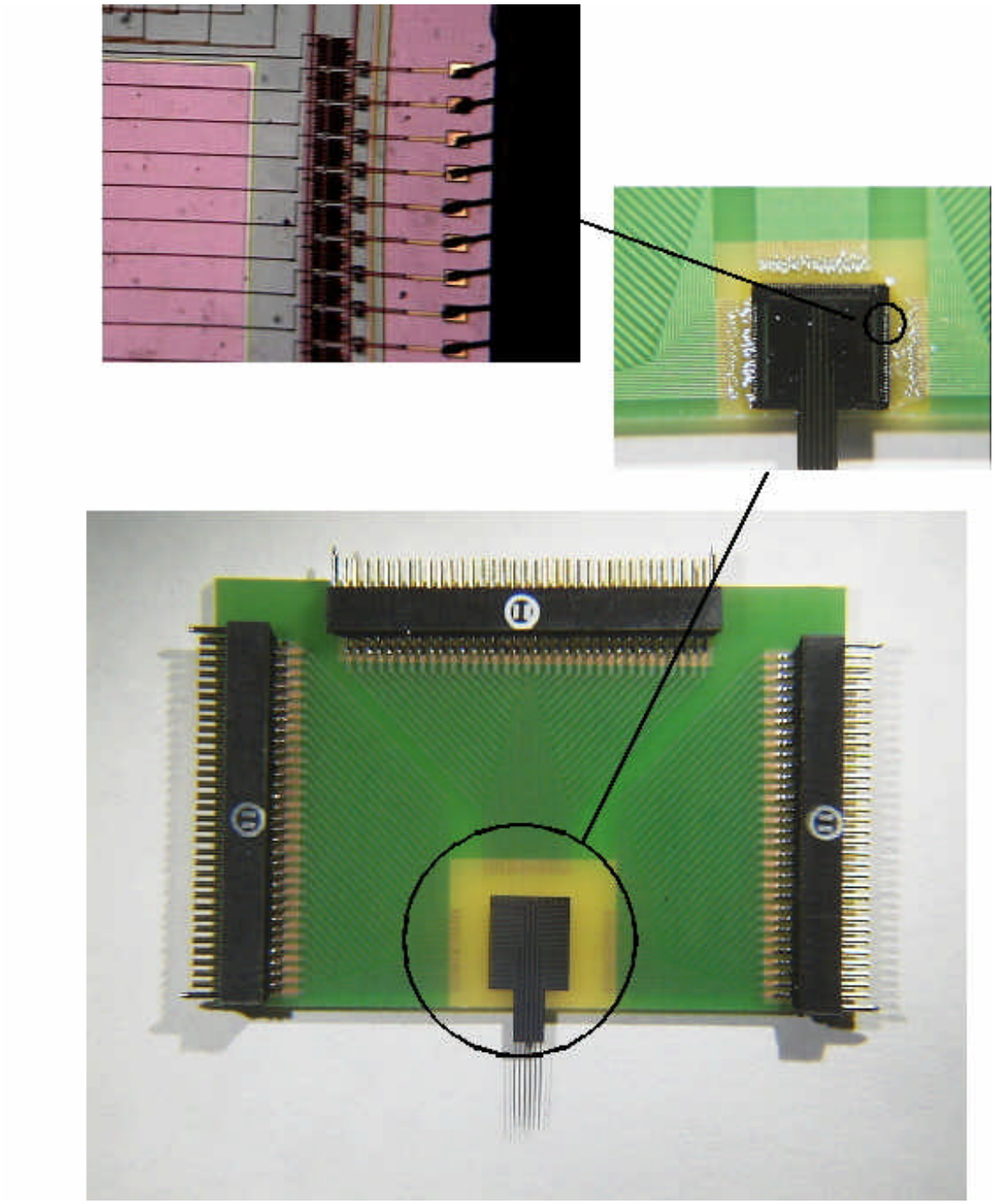


Fig. 5: Photograph of a bonded 96-site buffered recording probe with detail of wire bonds and on-chip buffer circuitry.

6. Amplifier Optimization for Use in Extracellular Recording

One of the key circuit blocks for use on all of our active probes is the recording amplifier. This circuit must be small, low-power, and robust, providing a known gain that is stable in the face of process variations. It must also provide input bias stabilization in the face of dc potential variations from the recording site and/or a significant gain in the signal passband and a very much lower gain at dc. A new amplifier meeting these criteria and suitable for neural recording applications has been designed and is shown in Fig. 6 below.

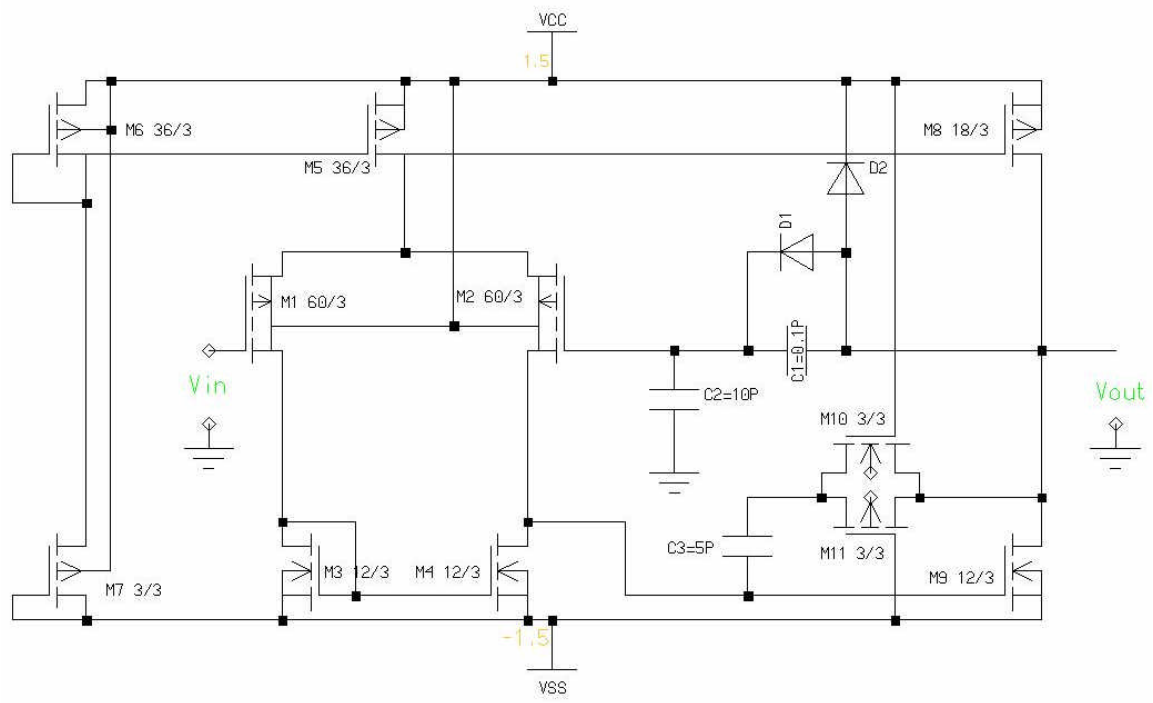


Fig. 6: Closed-Loop Amplifier Schematic

The amplifier pictured is a standard two-stage op-amp. It features a new diode capacitor feedback scheme that sets the passband gain of the amplifier and attenuates the low-frequency components of the neural signal. The frequency response of the amplifier is pictured in Fig. 7, and the transient response of the amplifier to a 100μV 1kHz input sinusoid is shown in Fig. 8. The mid-band gain of the amplifier is determined by the ratio C2/C1 and is set in this case to 100 (40db). The low-frequency pole seen in Fig. 7 is set by capacitance, C1, and the resistance seen across the sub-threshold-biased diode, D1, while the upper cut-off frequency is set by the Miller Capacitance, C3. Diode, D2, is formed between the n-epi layer and the p-well used to isolate diode, D1. D2 has been included in the analysis to ensure proper operation of the circuit upon fabrication.

The feedback configuration of this amplifier offers several advantages over previous implementations. First, the gain of the amplifier is nearly immune to threshold shifts, varying from 97.55 (39.8db) to 99.12 (39.9db) for ±25% threshold shifts.

Secondly, this feedback configuration does not require large current drive or static power dissipation. This can been seen by investigating the impedance of the feedback capacitor, C1. The equivalent resistance of C1 is 1.6G at 1kHz and is infinite at DC. This high impedance allows for very low current levels even for large output voltage swings. It is difficult to fabricate integrated resistors of this magnitude and even if fabrication were possible the thermal noise associated with such a large resistance would render them useless here. Thus, this amplifier is able to achieve a very stable gain without the added power consumption typically associated with resistive feedback schemes.

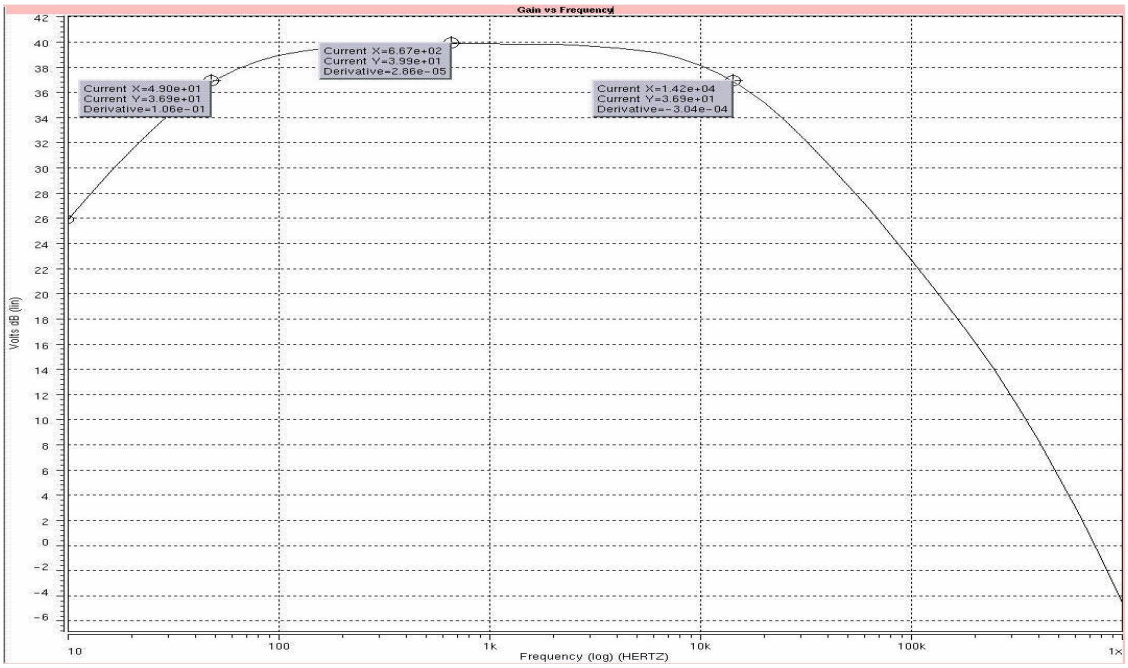


Fig. 7: AC response of the new neural recording amplifier

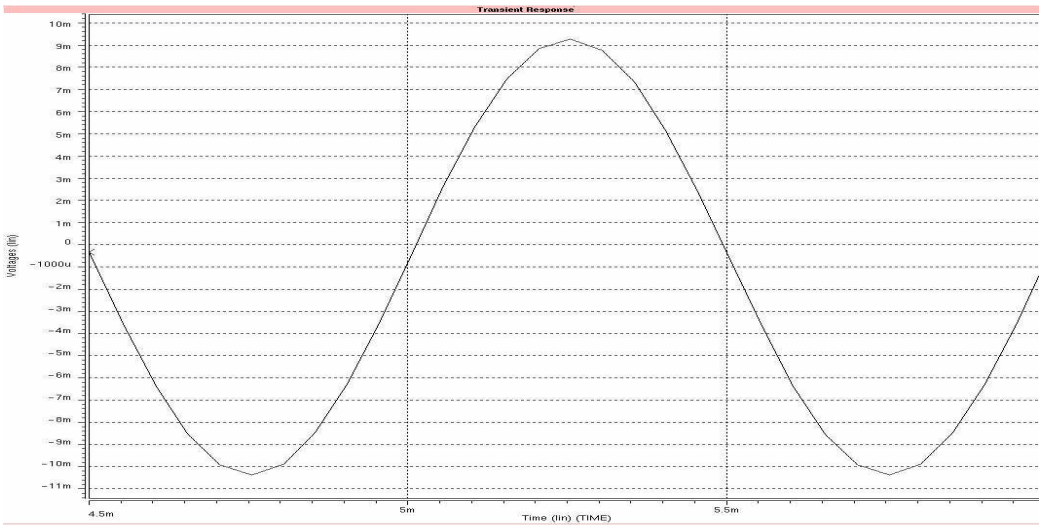


Fig. 8: Transient response to a 100µV 1KHz input signal.

The amplifier has been exhaustively simulated and a table listing the amplifier specifications is presented below. The amplifier displays a nominal gain of 98.4, 39.9db, and a passband from 46Hz to 14kHz. Furthermore, the DC gain of the amplifier is exactly unity and the AC gain varies from 97.7 to 98.1 as the dc input voltage shifts from –300mV to +300mV. The amplifier consumes 49μW of power from ±1.5V supplies and can be easily altered to operate from a 5V supply with a slight increase in power consumption. Additionally, the total integrated noise of the amplifier from 100Hz to 10KHz is 2.6μV rms.

Gain	39.9db
Passband	46Hz –14kHz
Power Dissipation	49μW
Input Referred Noise	2.6μV rms.

Table 1: Amplifier Specifications

The amplifier described here is currently in layout and fabrication should begin at the end of May. The major weakness of this amplifier is the large amount of area consumed by the capacitors C2 and C3. To overcome the problems associated with C2, a diode will be developed with a higher sub-threshold resistance than the diode modeled in our current process. This will allow C1 to be reduced without changing the low frequency cutoff of the amplifier. As C1 is reduced so will C2 be reduced to maintain the same gain. To reduce C3, while still maintaining the upper cutoff frequency, the gain will have to be increased. While increased gain is desirable, C2 will have to become larger, or C1 smaller, to achieve this. The key once again is to engineer the diode, D1, such that a small amplifier with all of the desirable qualities listed above can be achieved.

7. Design and Testing of an Integrated Telemetry System

As described in previous quarterly reports, the necessary circuit blocks for wireless operation of implantable recording microprobes have been designed and sent out for fabrication through the MOSIS foundry service. The test chip containing a number of these blocks was returned at the end of March, and is now ready for testing. Over the last quarter, work has been carried out on testing the front-end circuitry on this test chip and on designing the analog-to-digital converter for the final system.

7.1 The Telemetry Circuit Chip

Figure 9 shows the photograph of the fabricated chip. It contains circuit blocks for voltage regulation, a band-gap voltage reference, data detection, and clock recovery circuitry. Note that all of these circuit blocks are designed using a standard MOS process and are designed for low-power and high-performance operation. Simulation results for these circuit bocks were presented in previous progress reports and are not repeated here.

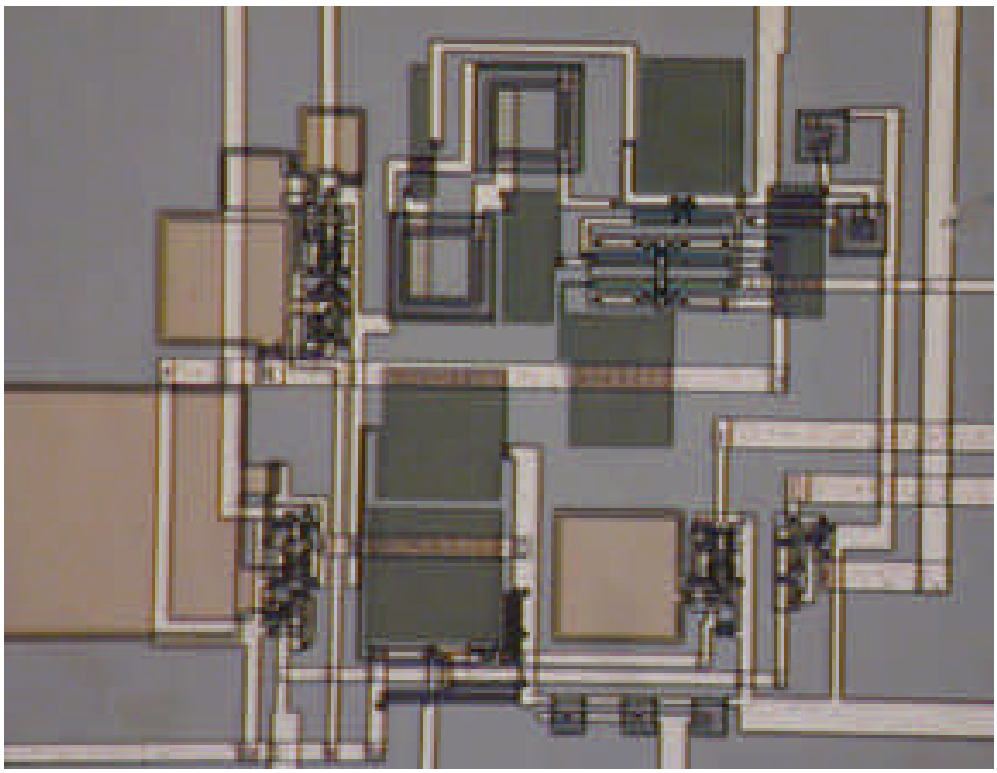


Fig. 9: Photograph of the fabricated telemetry chip.

Complete testing of the circuit chip has not yet been performed. Only preliminary testing of the band-gap reference voltage generator has been carried out. An external voltage of 5V was applied to the band-gap reference circuitry and the voltage reference V_{ref} was measured and found to match the SPICE simulation. The schematic of the band-gap circuitry was given in the last quarterly report. The accuracy and stability of this voltage reference are very important since it will be used as the input to the preceding amplifier in the voltage regulator. Complete testing of the telemetry chip will be performed on the chip in the next few weeks. A testing procedure has also been developed to fully characterize the circuit blocks before they are redesigned, if necessary, and incorporated into a complete system with amplifiers and analog-digital converters. The circuit blocks will be first tested using an rf signal produced and supplied via a hard-wired connection. These blocks will then be tested for wireless telemetry operation. Results from these tests will be presented in the next progress report.

7.2. Design of the Analog-Digital Converter (ADC)

One of the major circuit blocks in the final telemetry system is the analog-digital converter. There are several different architectures that can be potentially used to implement this circuit block. Each of the architectures has its specific advantages and disadvantages, as discussed below. During the past quarter, several of these architectures

were analyzed, with the aim of choosing the one best suited for this application. These architectures are briefly discussed below.

a) Integrating-type A/D converters

Integrating-type A/D converters, such as the ramp-integrating A/D converter, the dual-slope integrating A/D converter, and the voltage-to-frequency converter, are usually used in measuring and control systems having dc or slowly-varying analog signals. However, they are not suitable for this application, which requires a medium/high sampling speed.

b) Ramp and counter type and successive approximation A/Ds

Ramp and Counter type and successive approximation A/Ds are also considered but excluded due to relatively slow speed.

c) Full flash A/Ds

Full flash A/Ds use 2^N reference voltages and (2^N-1) voltage comparators. The speed of a full flash converter depends only on the speed of the analog comparator, making this kind of converter the fastest known. But the disadvantages include very high power dissipation, large chip area, and a large input capacitance. The resolution is limited by the accuracy of the reference voltage and comparator offset. Thus, it is often used in 6-8 bit applications if low-power operation is desired. Better performance can be obtained at the expense of a higher power dissipation. This is not desirable in this application and is therefore not being further pursued.

d) Pipelined parallel ADC architectures

It is widely believed that the pipelined architecture is the best approach to high-frequency high-resolution low-power ADCs in CMOS technology. State-of-the-art pipelined A/Ds can achieve 10 to 12 effective bits of resolution at speeds of 10 to 100MHz. Therefore, pipelined architecture is believed to be the best choice for this application. The schematic of a pipelined ADC is shown in Fig. 10.

The converter consists of a cascade of k stages, each comprising an S/H amplifier, a low resolution m-bit coarse ADC (sub-ADC), an m-bit DAC (sub-DAC), and an inter-stage gain block. In operation, each stage initially samples and holds the output from the previous stage and then the held input is converted into a low-resolution digital code by the sub-DAC. Finally, the inter-stage amplifier amplifies the difference between residue for the next stage. The use of S/H allows each stage to operate concurrently giving very high-speed conversion. The speed of a pipelined ADC is limited by the settling of the interstage S/H amplifier, so special consideration is necessary when designing this amplifier.

The main advantage of pipelined ADCs is the use of digital error correction to relax the linearity requirement of the sub-ADC to an m-bit level (i.e., stage resolution level) making the converter resolution dependent solely on the accuracy of the sub-DAC. The design of the m-bit ADC can be one of several current ADC architectures since the resolution requirements are significantly relaxed.

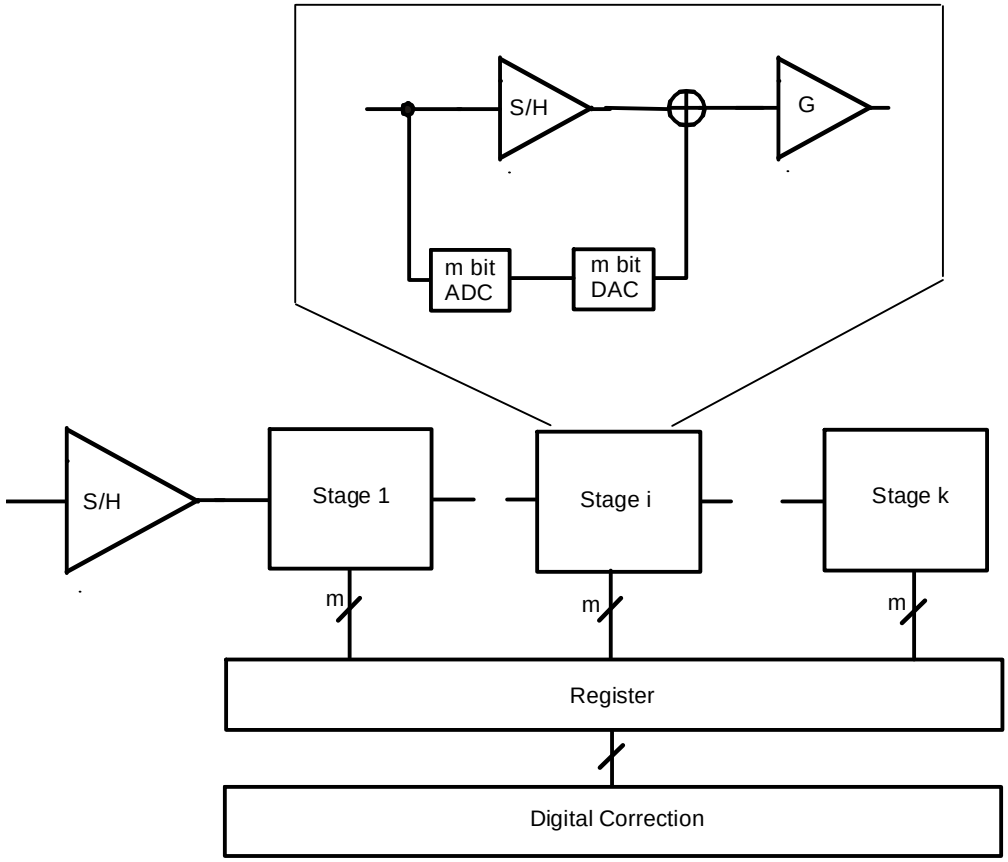


Fig. 10: Schematic of the pipelined parallel ADC architecture.

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e) Delta-Sigma Oversampled A/D Converters

Oversampled delta-sigma A/D converters have in recent years become more prevalent for high-accuracy, 12-bit to beyond 20-bit, A/D conversion of DC through moderately high (hundreds of kilohertz) AC signals. Their greatest advantage is that they trade greatly reduced analog circuit accuracy requirements for increased digital circuit complexity. The principle of delta-sigma A/D converter is shown in Fig. 11.

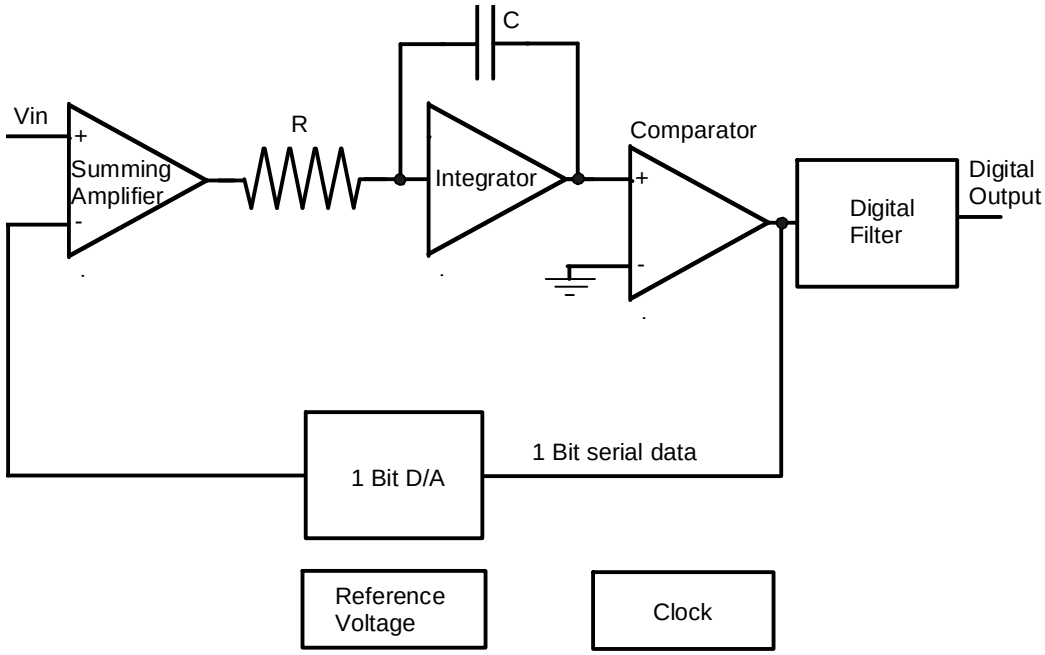

Fig. 11: Schematic of the delta-sigma A/D converter.

This converter only requires a single-bit A/D and a D/A converter with a relatively inaccurate differential summing amplifier and integrator (low-pass filter). These analog circuits are much easier to implement in a digital VLSI circuit than the accurate analog circuits required in parallel and successive approximation A/D converters that require precision resistors and capacitors.

Some low-power supply, low-power dissipation and high-accuracy delta-sigma A/D designs have been reported in the past several years [1-3]. In reference [1], 40μW of power consumption was reported at a sampling frequency of 1.538MHz and supply voltage of 900mV in a chip area of $0.85mm^2$. In summary, ΔΣ A/D converters and parallel architectures are good strategies for use in neural recording systems.

In the next quarter, we will choose the best ADC architecture and will complete the design and simulation of this circuit block for inclusion into a complete system. In addition, the telemetry circuit blocks will be completely tested and characterized for use in the complete telemetry system that will be designed and submitted for fabrication through MOSIS.

8. Conclusions

During the past quarter, we have begun a concerted effort to understand the chronic behavior of thin-film recording sites and its relationship to site processing, position, and design. Cleaning procedures are being explored via a series of chronic implants along with experiments investigating site position and size with respect to recording performance. Edge-mounted sites have recently shown high-quality recording performance to beyond 70 days in contrast to much more limited lifetimes typically seen for sites positioned in the center of the flat probe substrate. A series of recording probes having edge- and center-positioned sites have been fabricated and are now ready for implantation. These will allow a direct comparison with the two placements as well as a comparison with microwire electrodes.

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References:

[1] Vincenzi Peluso et al, “A 900-mV low power ΔΣ A/D converter with 77-dB Dynamic range” *IEEE Journal of Solid State Circuits*, Vol.33, No. 12, Dec, 1998

[2] S. Au and B.H. Leung, " A 1.95-v, 0.34-mW, 12-b sigma-delta modulator stablized by local feedback loops" *IEEE J. Solid-state Circuits*, Vol. 32, pp. 321-328, Mar. 1997

[3] S. Rabii and B. A. Wooley, "A 1/8V, 5.4 mW, digital-audio sigma-delta modulator in 1.2μm CMOS", in *Proc. Int. Solid-State Circuits Conf.*, Feb. 1996, pp. 228-229.